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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,707	11/11/2003	Luan C. Tran	MIO 0100 VA/40509.274/01-	6237

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,707	TRAN ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35* is/are allowed.

6)☒ Claim(s) *1-11,13-18,20-25,27-34 and 36-42* is/are rejected.

7)☒ Claim(s) *12,19 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 11 November 2003 is acceptable.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

2. **Claims 3 and 8** are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of claims 3 and 8 recites "said first source/drain region" which lacks an antecedent basis. Perhaps each of claims 2 and 4, from which claims 3 and 8 depend, should recite, instead of "forming a transistor in said active area", forming a transistor including a first source/drain region and a second source/drain region in said active area.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 2-3, 34, and 39** are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. U.S. Patent 5,840,591 (the '591 patent).

The '591 patent discloses in Figures 4 through 10's and respective portions of the specification a method of making a memory cell as claimed.

Referring to **claims 39, 2, and 34**, the '591 patent discloses a method of making a memory cell comprising:

providing a base substrate 100 having an uppermost surface;

forming a strip of active area (no number, defined generally by the area that transistors will be formed) on said uppermost surface of said base substrate;

forming a plurality of pairs of transistors in said strip of active area, each of said pairs of transistors sharing a common first source/drain region 126 or 126' and further comprising a channel (no number) separated between said common first source/drain region[;] and a second source/drain region 126 or 126';

coupling a word line (not shown but must be present for the device to function) to said channel of each transistor defining a transistor gate 122 (Figure 9A).

etching a trench 103 in said base substrate generally along side and adjacent to said strip of active area;

lining at least a portion of the walls of said trench with a spacer 105 (Figure 7B);

depositing a conductive bit line 106 over said substrate at least within said trench (Figure 8B);

etching said conductive bit line back such that said conductive bit line is recessed below said uppermost surface of said base substrate 100 (Figure 8B and column 5, lines 14-17);

forming a cap 108 ("third insulating layer") within said trench over said conductive bit line 106;

forming a plurality of bit line contact straps 130 (Figure 9B, although only one is shown), each bit line contact strap coupled between said conductive bit line 106 and an associated one of said common first source/drain regions of said transistor at least about said uppermost surface of said substrate (Figures 9A *and* 9B);

forming a plurality of capacitors over said substrate; and

electrically coupling each capacitor to an associated one of said second source/drain region (through contact 136, Figure 10A, and paragraph bridging columns 5 and 6).

Referring to **claim 3**, the '591 patent further discloses comprising coupling said bit line strap 130 (Figure 9B) to said first source/drain region 126' through said side wall of said trench.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1, 36, and 40-42** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '591 patent.

Referring to **claims 40 and 41**, it is within the skill of one in the art at the time the invention was made to change the method disclosed by the '591 patent and detailed above including forming a plurality of pairs of transistors to include forming a first source/drain region,

a first channel, a second source/drain region, a second channel, a third source/drain region, a third channel, a fourth source/drain region, a fourth channel, a fifth source/drain region, a fifth channel and a sixth source/drain region; and to include coupling a first conductive layer to said third channel and coupling said first conductive layer to a ground reference voltage.

Referring to **claim 42**, it is within the skill of one in the art at the time the invention was made to utilize the memory cell disclosed by the '591 patent and detailed above in forming a memory device of a computer system, which is formed by providing a processor, providing a storage device communicably coupled to said processor, providing at least one input/output device communicably coupled to said processor, and providing the memory device.

With reference to the limitation "at least a first distance sufficiently deep to substantially avoid gate induced drain leakage effects" of **claims 1 and 36**, it appears that the distance, defined by etching back the buried bit line (BBL) 106 as disclosed by the '591 patent, is sufficiently deep to substantially avoid gate induced drain leakage effects. There is simply no evidence that the device produced by the process disclosed by the '591 patent will not function as claimed.

5. **Claims 4-11, 13-25, 27-33, and 37-38** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '591 patent in view of Shen U.S. Patent 6,537,870 (the '870 patent).

Referring to **claims 4-8, 10, 11, 18, 25, 30, 31, 33, 37, and 38**, the '591 patent discloses a method of making a memory cell including a capacitor storage node (DRAM) as claimed and as detailed above, but providing a base substrate 100 instead of providing a base substrate having a first base layer and a second base layer, providing a base substrate 100 instead of providing a

base substrate having an a first base layer of semiconductor material formed over a second base layer of an insulating material, and providing a base substrate 100 instead of providing a base substrate having an uppermost surface then forming a first type well within said base substrate.

The '870 patent, in disclosing a method for forming a DRAM structure having BBL and self-aligned trenches, teaches that memory cells are formed in silicon region 102, which could be a silicon substrate just as disclosed by the '591 patent, or a semiconductor region over or within another semiconductor region, e.g., an epitaxial layer or a well (or tub or tank), or a semiconductor layer grown over an insulator (e.g., silicon-over-insulator ("SOI") or silicon-over sapphire) (last full paragraph of column 4), thereby teaching that these different kinds of base substrates are art-recognized equivalent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the manufacturing methods of the '591 patent to include providing a base substrate having a first base layer and a second base layer, or to include providing a base substrate having an a first base layer of semiconductor material formed over a second base layer of an insulating material, or to include providing a base substrate having an uppermost surface then forming a first type well within the base substrate. One would have been motivated to make such a modification in view of the suggestion in the '870 patent that the various claimed base substrates are art-recognized equivalents.

Referring to the limitation "etching a trench in said base substrate passing generally adjacent to said transistor" of **claims 18 and 25**, although the modified method detailed above teaches forming the trench in the base substrate then forming the transistor, there is simply no evidence in the specification of the present invention that articulates one order of steps over the

other. Therefore, the different orders of steps are just different ways one of ordinary skill in the art would perform in forming trenches.

With respect to **claims 9, 17, 24, 29, and 32**, the modified method detailed above further comprises coupling said bit line strap 130 (Figure 9B) to said first source/drain region 126' through said side wall of said trench.

Referring to **claims 13, 20, and 27**, the trench of the modified method as detailed above is etched to a depth (about 400nm – column 4, lines 62-63) greater than twice a minimum reliable feature size (about 150nm at the time of the invention).

Regarding the different steps and characteristics for forming the spacer and capping layer of **claims 14-16, 21-23, and 28**, although the '591 patent discloses only oxide or nitride as the trench spacer (liner) or capping layer, the use of oxide and/or nitride as trench liners and capping layers was known in the art and was therefore obvious at the time the invention was made. See, for example, U.S. Patent 6,573,137 to Divakaruni et al., which details the use of oxide and nitride as trench liners/spacers and capping layers.

Allowable Subject Matter

6. **Claim 35** is allowable over the prior art of record.

Claims 12, 19, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all

limitations are considered within the claimed specific combination, fails to teach or render obvious a method of making a memory cell having all exclusive limitations as recited in claims 35, 11/12, 18/19, and 25/26, characterized in that the conductive bit line is recessed below the uppermost surface of the base substrate by at least a first distance defined by the combined distances of a junction depth plus a depletion width of the transistor.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

TH

Tu-Tu Ho
March 04, 2004

David Nelms
Supervisory Patent Examiner
Technology Center 2800